SHUYANG LI

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EDUCATION

Georgia Institute of Technology *August 2025 - June 2030 (expected)*
Ph.D. in Electrical and Computer Engineering

Fudan University *September 2020 - June 2025*
B.S. in Microelectronic Science and Engineering
Overall GPA: 3.85/4.0

KTH Royal Institute of Technology *January 2022 - July 2022*
Exchange student, EECS School
Achieved Grade A (Excellence) in All Courses

RESEARCH INTERESTS

Computer Architecture, Hardware/Software Co-design, FPGAs, High Level Synthesis (HLS), Domain-specific Accelerator, Machine Learning (ML) for Eletronic Design Automation (EDA)

PUBLICATIONS

S. Li, H. Zhang, R. Chen, C. Hao, "TrackGNN: A Highly Parallelized and FIFO-Balanced GNN Accelerator for Track Reconstruction on FPGAs," *The 33th IEEE International Symposium on Field-Programmable Custom Computing Machines (FCCM 2025)*. **Status: Published** [Paper]DOI: 10.1109/FCCM62733.2025.00029

Y. Liu, **S. Li**, R. Chen, Y. Li, J. Yu, K. Wang, "DIF-LUT Pro: An Automated Tool for Simple yet Scalable Approximation of Nonlinear Activation on FPGA," *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems (TCAD)*. **Status: Published**[Paper]DOI: 10.1109/TCAD.2025.3576333

Y. Liu, R. Chen, **S. Li**, J. Yang, S. Li, B. da Silva, "FPGA-Based Sparse Matrix Multiplication Accelerators: From State-of-the-art to Future Opportunities," *ACM Transactions on Reconfigurable Technology and Systems (TRETS)*, 2024. **Status: Published** [Paper]DOI: 10.1145/3687480

X. Zhou, **S. Li**, H. Lu, K. Wang, "PipeFuser: Building Flexible Pipeline Architecture for DNN Accelerators via Layer Fusion," *The 29th Annual International Conference on VLSI Design Automation in Asia and South Pacific Regions (ASP-DAC 2024)*, Incheon Songdo Convensia, South Korea, January 22-25, 2024. **Status: Published** [Paper]DOI: 10.1109/ASP-DAC58780.2024.10473790

S. Li, X. Zhou, H. Lu, K. Wang, "DNNMapper: an Elastic Framework for Mapping DNNs to Multi-Die FPGAs," *2024 IEEE International Symposium on Circuits and Systems (ISCAS 2024)*, Singapore, May 19-22, 2024. **Status: Published** [Paper]DOI: 10.1109/ISCAS58744.2024.10558120

RESEARCH EXPERIENCE

Software/Hardware Co-design Lab (Sharc), Georgia Institute of Technology Atlanta, Georgia
Ph.D. student (formerly Undergraduate Research Intern) *April 2024 - Present*

- Supervised by Professor Cong (Callie) Hao.
- Contributed to the optimization of **TrackGNN**, a highly parallelized and self-adaptive accelerator for track reconstruction on FPGAs.
- Led ongoing efforts to extend TrackGNN with improved parallelism and scalability, contributed to experimental design and manuscript. [github]

Computer Systems Laboratory, Cornell University Ithaca, New York
Undergraduate Research Intern *March 2024 - Feb 2025*

- Supervised by Professor Zhiru Zhang and Ph.D. Student Yixiao Du.
- Contributed to the design and implementation of a hardware accelerator for diffusion language model based on HLS and the Allo framework.[1]

FOXKEN-AI LAB, Fudan University Shanghai, China
Undergraduate Student Researcher *December 2021 - August 2024*

- **DIF-LUT Pro: An Automated Tool for Simple yet Scalable Approximation of Nonlinear Activation on FPGA**

March 2024 - August 2024

- Contributed as the second author.
- Conducted a performance evaluation study between entry numbers and key bits for the proposed approximation method.
- Contributed to mathematical formulations and preliminaries in the manuscript.
- **FPGA-Based Sparse Matrix Multiplication Accelerators: From State-of-the-art to Future Opportunities**

November 2023 - May 2024

- Contributed to the review of FPGA-Based sparse matrix multipliers.
- **PipeFuser: Building Flexible Pipeline Architecture for DNN Accelerators via Layer Fusion**

March 2023 - July 2023

- Implemented a fused-pipeline architecture for DNN accelerator to overcome the drawbacks of full-pipeline and non-pipeline architectures.
- Designed an end-to-end framework, PipeFuser, for efficient architecture implementation.
- Contributed to the Co-design Engine based on a genetic algorithm (GA) for fused-pipeline Design Space Exploration (DSE) in PipeFuser.
- **DNNMapper: an Elastic Framework for Mapping DNNs to Multi-Die FPGAs** March 2023 - October 2023
- Contributed as the first author.
- Proposed an automated framework for mapping DNNs to multi-die FPGAs with improved resource allocation, timing quality and greater flexibility.

STANDARDIZED TEST SCORES

GRE (General Test): Verbal: 155, Quant: 168, Writing: 3.5
TOEFL: Overall: 104 (R: 27, L: 30, S: 23, W: 24)

TECHNICAL STRENGTHS

Programming Languages	C/C++, Python, High-Level Synthesis (HLS), Verilog HDL
EDA Tools	Vivado, Vitis, HSPICE, Design Compiler
Machine Learning Framework	Pytorch, Paddle, Tensorflow
Math-related Softwares	Matlab, Origin
Collaboration and Documentation	Latex, Visio, Git, Markdown, Google Colab, Notion, Overleaf

[1] Chen H, Zhang N, Xiang S, et al. Allo: A Programming Model for Composable Accelerator Design[J]. Proceedings of the ACM on Programming Languages, 2024, 8(PLDI): 593-620.